SEMI China CSM Std. Technical Committee

SiC Epitaxial Wafer Task Force

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Dec. 5, 2024

STANDARDS

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15	嵇青胜 Bovey	瑟米莱伯贸易（上海）有限公司 Semilab Trade（Shanghai）Co., Ltd.	Instrument &Equipment 仪器&设备	2023Q4新加入工作组

Documents in Work

SEMI Draft Document: 4H-SiC homo-epitaxial wafer Specification 4H-SiC同质外延片标准

➢ Progress of Documents Work 标准工作进展

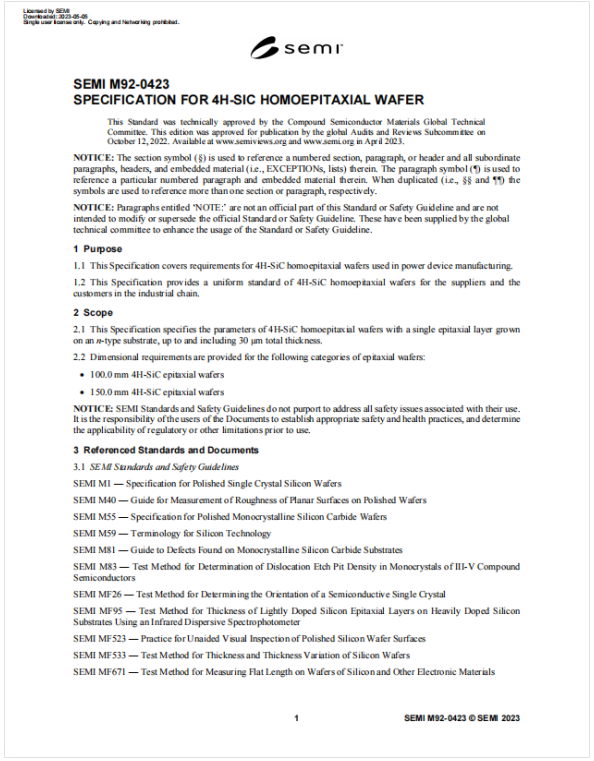
- **Jan. 2022:** Passed the first cycle voting by SEMI Global Compound Semiconductor Technical Committee(通过semi化合物半导体标准技术委员会第一轮全球投票）.
- **Jun. 2022:** Passed SEMI ISC Audits & Reviews SubCommittee review （通过SEMI ISC Audits & Reviews SubCommittee 审阅）.
- **Jul. 2022:** Passed ratification ballot（通过全球补充投票阶段）.
- **Oct. 2022:** Passed A&R review stage, publication pending（通过A&R审阅，现正等待正式发布中）.
- Apr. 2023 Published. 正式发布.

semi STANDARDS

Documents in Work

SEMI Draft Document (Published): M092-0423 4H-SiC Homoepitaxial Wafer

Specification 4H-SiC同质外延片标准



SEMI M92-0423
SPECIFICATION FOR 4H-SIC HOMOEPITAXIAL WAFER

This Standard was technically approved by the Compound Semiconductor Materials Global Technical Committee. This edition was approved for publication by the global Audits and Reviews Subcommittee on October 12, 2022. Available at www.semiviews.org and www.semi.org in April 2023.

NOTICE: The section symbol (§) is used to reference a numbered section, paragraph, or header and all subordinate paragraphs, headers, and embedded material (i.e., EXCEPTIONs, lists) therein. The paragraph symbol (¶) is used to reference a particular numbered paragraph and embedded material therein. When duplicated (i.e., §§ and ¶¶) the symbols are used to reference more than one section or paragraph, respectively.

NOTICE: Paragraphs entitled 'NOTE:' are not an official part of this Standard or Safety Guideline and are not intended to modify or supersede the official Standard or Safety Guideline. These have been supplied by the global technical committee to enhance the usage of the Standard or Safety Guideline.

1 Purpose

1.1 This Specification covers requirements for 4H-SiC homoepitaxial wafers used in power device manufacturing.

1.2 This Specification provides a uniform standard of 4H-SiC homoepitaxial wafers for the suppliers and the customers in the industrial chain.

2 Scope

2.1 This Specification specifies the parameters of 4H-SiC homoepitaxial wafers with a single epitaxial layer grown on an *n*-type substrate, up to and including 30 µm total thickness.

2.2 Dimensional requirements are provided for the following categories of epitaxial wafers:

- 100.0 mm 4H-SiC epitaxial wafers
- 150.0 mm 4H-SiC epitaxial wafers

NOTICE: SEMI Standards and Safety Guidelines do not purport to address all safety issues associated with their use. It is the responsibility of the users of the Documents to establish appropriate safety and health practices, and determine the applicability of regulatory or other limitations prior to use.

3 Referenced Standards and Documents

3.1 *SEMI Standards and Safety Guidelines*

SEMI M1 — Specification for Polished Single Crystal Silicon Wafers

SEMI M40 — Guide for Measurement of Roughness of Planar Surfaces on Polished Wafers

SEMI M55 — Specification for Polished Monocrystalline Silicon Carbide Wafers

SEMI M59 — Terminology for Silicon Technology

SEMI M81 — Guide to Defects Found on Monocrystalline Silicon Carbide Substrates

SEMI M83 — Test Method for Determination of Dislocation Etch Pit Density in Monocrystals of III-V Compound Semiconductors

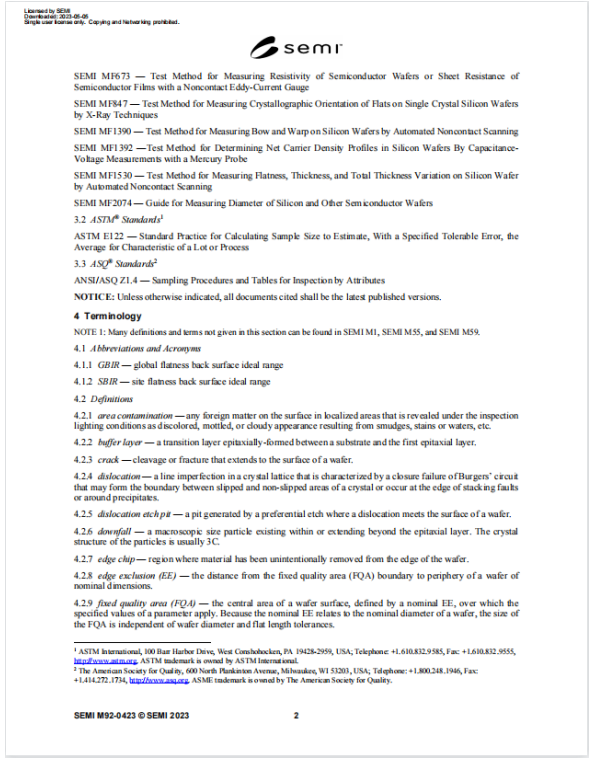
SEMI MF26 — Test Method for Determining the Orientation of a Semiconductive Single Crystal

SEMI MF95 — Test Method for Thickness of Lightly Doped Silicon Epitaxial Layers on Heavily Doped Silicon Substrates Using an Infrared Dispersive Spectrophotometer

SEMI MF523 — Practice for Unaided Visual Inspection of Polished Silicon Wafer Surfaces

SEMI MF533 — Test Method for Thickness and Thickness Variation of Silicon Wafers

SEMI MF671 — Test Method for Measuring Flat Length on Wafers of Silicon and Other Electronic Materials



SEMI MF673 — Test Method for Measuring Resistivity of Semiconductor Wafers or Sheet Resistance of Semiconductor Films with a Noncontact Eddy-Current Gauge

SEMI MF847 — Test Method for Measuring Crystallographic Orientation of Flats on Single Crystal Silicon Wafers by X-Ray Techniques

SEMI MF1390 — Test Method for Measuring Bow and Warp on Silicon Wafers by Automated Noncontact Scanning

SEMI MF1392 — Test Method for Determining Net Carrier Density Profiles in Silicon Wafers By Capacitance-Voltage Measurements with a Mercury Probe

SEMI MF1530 — Test Method for Measuring Flatness, Thickness, and Total Thickness Variation on Silicon Wafer by Automated Noncontact Scanning

SEMI MF2074 — Guide for Measuring Diameter of Silicon and Other Semiconductor Wafers

3.2 *ASTM® Standards*[1]

ASTM E122 — Standard Practice for Calculating Sample Size to Estimate, With a Specified Tolerable Error, the Average for Characteristic of a Lot or Process

3.3 *ASQ® Standards*[2]

ANSI/ASQ Z1.4 — Sampling Procedures and Tables for Inspection by Attributes

NOTICE: Unless otherwise indicated, all documents cited shall be the latest published versions.

4 Terminology

NOTE 1: Many definitions and terms not given in this section can be found in SEMI M1, SEMI M55, and SEMI M59.

4.1 *Abbreviations and Acronyms*

4.1.1 *GBIR* — global flatness back surface ideal range

4.1.2 *SBIR* — site flatness back surface ideal range

4.2 *Definitions*

4.2.1 *area contamination* — any foreign matter on the surface in localized areas that is revealed under the inspection lighting conditions as discolored, mottled, or cloudy appearance resulting from smudges, stains or waters, etc.

4.2.2 *buffer layer* — a transition layer epitaxially-formed between a substrate and the first epitaxial layer.

4.2.3 *crack* — cleavage or fracture that extends to the surface of a wafer.

4.2.4 *dislocation* — a line imperfection in a crystal lattice that is characterized by a closure failure of Burgers' circuit that may form the boundary between slipped and non-slipped areas of a crystal or occur at the edge of stacking faults or around precipitates.

4.2.5 *dislocation etch pit* — a pit generated by a preferential etch where a dislocation meets the surface of a wafer.

4.2.6 *downfall* — a macroscopic size particle existing within or extending beyond the epitaxial layer. The crystal structure of the particles is usually 3C.

4.2.7 *edge chip* — region where material has been unintentionally removed from the edge of the wafer.

4.2.8 *edge exclusion (EE)* — the distance from the fixed quality area (FQA) boundary to periphery of a wafer of nominal dimensions.

4.2.9 *fixed quality area (FQA)* — the central area of a wafer surface, defined by a nominal EE, over which the specified values of a parameter apply. Because the nominal EE relates to the nominal diameter of a wafer, the size of the FQA is independent of wafer diameter and flat length tolerances.

[1] ASTM International, 100 Barr Harbor Drive, West Conshohocken, PA 19428-2959, USA; Telephone: +1.610.832.9585, Fax: +1.610.832.9555, http://www.astm.org. ASTM trademark is owned by ASTM International.
[2] The American Society for Quality, 600 North Plankinton Avenue, Milwaukee, WI 53203, USA; Telephone: +1.800.248.1946, Fax: +1.414.272.1734, http://www.asq.org. ASME trademark is owned by The American Society for Quality.

4.2.10 *global flatness back surface ideal range (GBIR)* — a parameter of flatness.

4.2.10.1 *Discussion* — Refer to SEMI M1, Appendix 1, Flatness Decision Tree. Formerly also known as 'total thickness variation (TTV)'.

4.2.11 *homoepitaxial layer* — thin monocrystalline film epitaxially-formed on a substrate of the same material and crystallographic orientation, inheriting the atomic order of the substrate.

4.2.12 *micropipe* — small hollow tube basically parallel to the crystallographic c-axis and extending typically through larger parts of the crystal boule and thus affecting several neighboring wafers. Micropipes may be generated at bulk defects, for example, inclusions, polytype defects or crystallites. (Refer to SEMI M81 for examples.)

4.2.13 *polytype* — one of the modifications of monocrystalline material which shows polytypism.

4.2.14 *polytypism* — phenomenon where a material occurs in several structural modifications, each of which can be regarded as built up by stacking layers of identical structure and chemical composition.

4.2.15 *site flatness back surface ideal range (SBIR)* — a parameter of flatness.

4.2.15.1 *Discussion* — Refer to SEMI M1, Appendix 1, Flatness Decision Tree. Formerly also known as 'local thickness variation (LTV or LTVmax)'.

4.2.16 *scratch* — a shallow groove or cut below the established plane of the surface of a semiconductor wafer, with a length to width ratio greater than 5:1.

4.2.17 *silicon carbide (SiC)* — semiconductor crystal composed of silicon and carbon, which will exhibit a large number of polytypes such as 3C, 4H, 6H, and 15R.

NOTE 2: A symbol like 4H- gives the number of periodic stacking bilayers (2, 3, 4...) and the crystal symmetry (H = hexagonal, C = cubic, and R = Rhombohedral) of each polytype.

4.2.18 *substrate* — a wafer that is the basis for subsequent processing operations in the fabrication of semiconductor devices or circuits that may be fabricated directly in the substrate or in a film of the same or another material grown or deposited on the substrate.

4.2.19 *surface killer defect* — surface killer defects of 4H-SiC epitaxial wafers caused by epitaxial growth are including downfall, triangular defect and carrot defect.

4.2.20 *total usable area* — the proportion of the area of the wafer without surface killer defects to the area of the entire wafer.

4.2.21 *triangular defect* — a triangle-shaped defect on the 4H-SiC epitaxial layer surface, which is a lamellar inclusion with a cubic (3C) stacking sequence, so-called '3C inclusion', extending toward the epitaxial layer surface.

5 Ordering Information

5.1 Purchase orders for 4H-SiC epitaxial wafers furnished to this Specification shall include the following items from substrate, buffer layer and epitaxial layer. In addition, the purchase order must indicate the test method to be used in evaluating each of the specified items for which alternate test procedures exist. Special requirements of ordering information shall be agreed upon between the supplier and the purchaser.

5.2 *Substrate*

5.2.1 Substrate Vendor,

5.2.2 Crystal Polytype,

5.2.3 Conductivity Type,

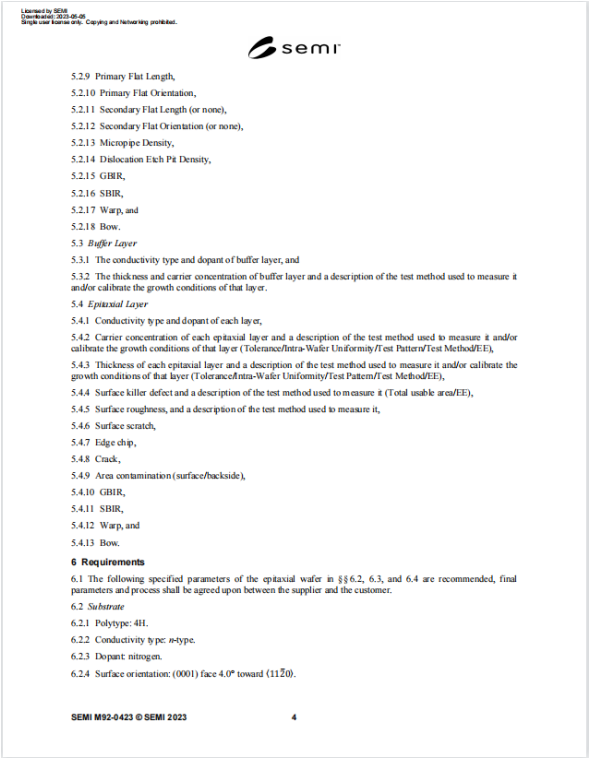
5.2.4 Dopant,

5.2.5 Diameter,

5.2.6 Thickness,

5.2.7 Wafer Surface Orientation,

5.2.8 Resistivity,



5.2.9 Primary Flat Length,

5.2.10 Primary Flat Orientation,

5.2.11 Secondary Flat Length (or none),

5.2.12 Secondary Flat Orientation (or none),

5.2.13 Micropipe Density,

5.2.14 Dislocation Etch Pit Density,

5.2.15 GBIR,

5.2.16 SBIR,

5.2.17 Warp, and

5.2.18 Bow.

5.3 *Buffer Layer*

5.3.1 The conductivity type and dopant of buffer layer, and

5.3.2 The thickness and carrier concentration of buffer layer and a description of the test method used to measure it and/or calibrate the growth conditions of that layer.

5.4 *Epitaxial Layer*

5.4.1 Conductivity type and dopant of each layer,

5.4.2 Carrier concentration of each epitaxial layer and a description of the test method used to measure it and/or calibrate the growth conditions of that layer (Tolerance/Intra-Wafer Uniformity/Test Pattern/Test Method/EE),

5.4.3 Thickness of each epitaxial layer and a description of the test method used to measure it and/or calibrate the growth conditions of that layer (Tolerance/Intra-Wafer Uniformity/Test Pattern/Test Method/EE),

5.4.4 Surface killer defect and a description of the test method used to measure it (Total usable area/EE),

5.4.5 Surface roughness, and a description of the test method used to measure it,

5.4.6 Surface scratch,

5.4.7 Edge chip,

5.4.8 Crack,

5.4.9 Area contamination (surface/backside),

5.4.10 GBIR,

5.4.11 SBIR,

5.4.12 Warp, and

5.4.13 Bow.

6 Requirements

6.1 The following specified parameters of the epitaxial wafer in §§6.2, 6.3, and 6.4 are recommended, final parameters and process shall be agreed upon between the supplier and the customer.

6.2 *Substrate*

6.2.1 Polytype: 4H.

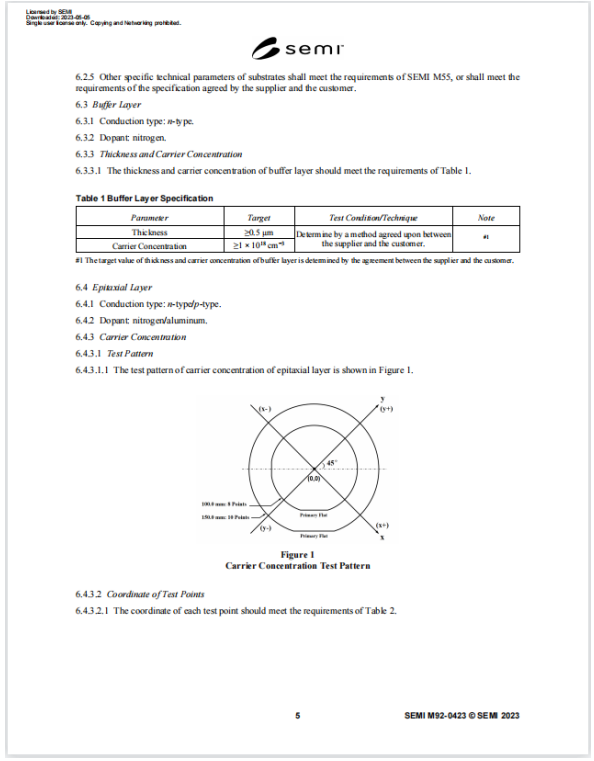
6.2.2 Conductivity type: *n*-type.

6.2.3 Dopant: nitrogen.

6.2.4 Surface orientation: (0001) face 4.0° toward $\langle 11\bar{2}0 \rangle$.

Documents in Work

SEMI Draft Document (Published): M092-0423 4H-SiC Homoepitaxial Wafer Specification 4H-SiC同质外延片标准



6.2.5 Other specific technical parameters of substrates shall meet the requirements of SEMI M55, or shall meet the requirements of the specification agreed by the supplier and the customer.

6.3 *Buffer Layer*

6.3.1 Conduction type: *n*-type.

6.3.2 Dopant: nitrogen.

6.3.3 *Thickness and Carrier Concentration*

6.3.3.1 The thickness and carrier concentration of buffer layer should meet the requirements of Table 1.

Table 1 Buffer Layer Specification

Parameter	*Target*	*Test Condition/Technique*	*Note*
Thickness	≥0.5 μm	Determine by a method agreed upon between the supplier and the customer.	#1
Carrier Concentration	≥1 × 10^{18} cm^{-3}		

#1 The target value of thickness and carrier concentration of buffer layer is determined by the agreement between the supplier and the customer.

6.4 *Epitaxial Layer*

6.4.1 Conduction type: *n*-type/*p*-type.

6.4.2 Dopant: nitrogen/aluminum.

6.4.3 *Carrier Concentration*

6.4.3.1 *Test Pattern*

6.4.3.1.1 The test pattern of carrier concentration of epitaxial layer is shown in Figure 1.

Figure 1
Carrier Concentration Test Pattern

6.4.3.2 *Coordinate of Test Points*

6.4.3.2.1 The coordinate of each test point should meet the requirements of Table 2.

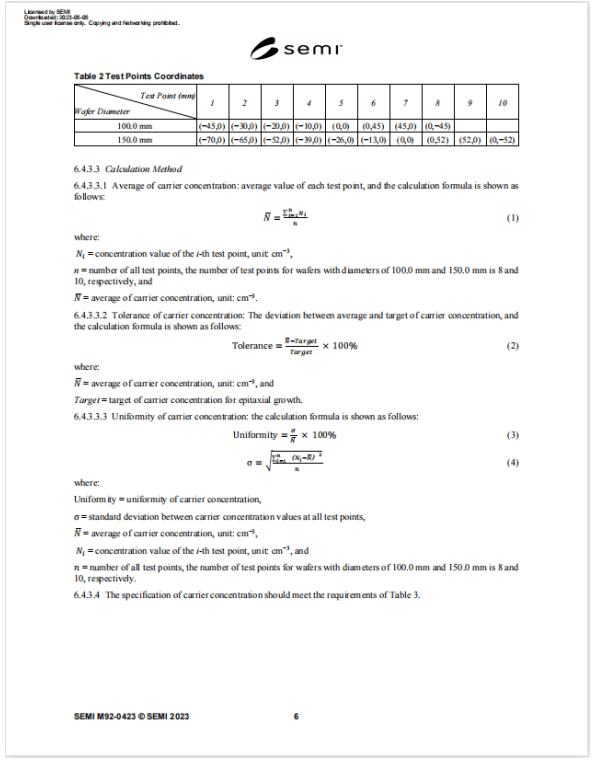


Table 2 Test Points Coordinates

Wafer Diameter \ *Test Point (mm)*	*1*	*2*	*3*	*4*	*5*	*6*	*7*	*8*	*9*	*10*
100.0 mm	(−45,0)	(−30,0)	(−20,0)	(−10,0)	(0,0)	(0,45)	(45,0)	(0,−45)		
150.0 mm	(−70,0)	(−65,0)	(−52,0)	(−39,0)	(−26,0)	(−13,0)	(0,0	(0,52)	(52,0)	(0,−52)

6.4.3.3 *Calculation Method*

6.4.3.3.1 Average of carrier concentration: average value of each test point, and the calculation formula is shown as follows:

$$\overline{N} = \frac{\sum_{i=1}^{n} N_i}{n} \quad (1)$$

where:

N_i = concentration value of the *i*-th test point, unit: cm^{-3},

n = number of all test points, the number of test points for wafers with diameters of 100.0 mm and 150.0 mm is 8 and 10, respectively, and

$\overline{N}$ = average of carrier concentration, unit: cm^{-3}.

6.4.3.3.2 Tolerance of carrier concentration: The deviation between average and target of carrier concentration, and the calculation formula is shown as follows:

$$\text{Tolerance} = \frac{\overline{N} - Target}{Target} \times 100\% \quad (2)$$

where:

$\overline{N}$ = average of carrier concentration, unit: cm^{-3}, and

Target = target of carrier concentration for epitaxial growth.

6.4.3.3.3 Uniformity of carrier concentration: the calculation formula is shown as follows:

$$\text{Uniformity} = \frac{\sigma}{\overline{N}} \times 100\% \quad (3)$$

$$\sigma = \sqrt{\frac{\sum_{i=1}^{n} (N_i - \overline{N})^2}{n}} \quad (4)$$

where:

Uniformity = uniformity of carrier concentration,

σ = standard deviation between carrier concentration values at all test points,

$\overline{N}$ = average of carrier concentration, unit: cm^{-3},

N_i = concentration value of the *i*-th test point, unit: cm^{-3}, and

n = number of all test points, the number of test points for wafers with diameters of 100.0 mm and 150.0 mm is 8 and 10, respectively.

6.4.3.4 The specification of carrier concentration should meet the requirements of Table 3.

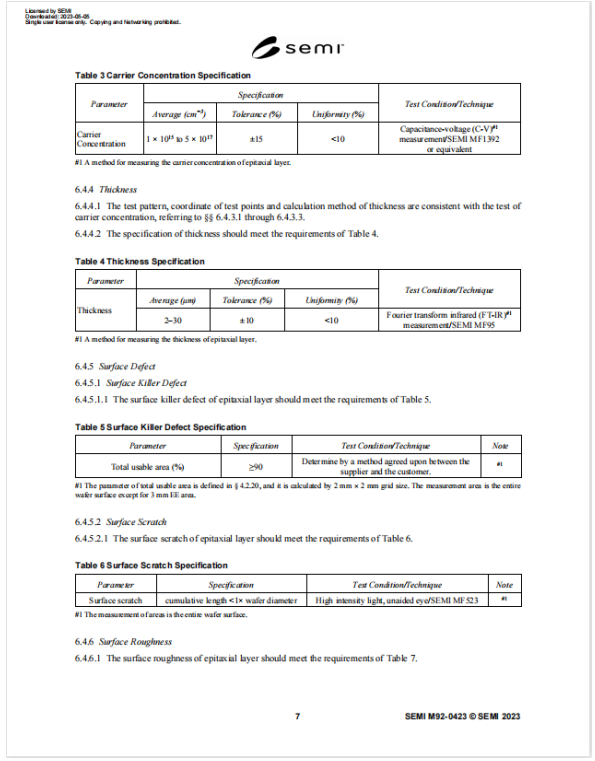


Table 3 Carrier Concentration Specification

Parameter	*Specification*			*Test Condition/Technique*
	Average (cm^{-3})	*Tolerance (%)*	*Uniformity (%)*	
Carrier Concentration	1 × 10^{15} to 5 × 10^{17}	±15	<10	Capacitance-voltage (C-V)#1 measurement/SEMI MF1392 or equivalent

#1 A method for measuring the carrier concentration of epitaxial layer.

6.4.4 *Thickness*

6.4.4.1 The test pattern, coordinate of test points and calculation method of thickness are consistent with the test of carrier concentration, referring to §§ 6.4.3.1 through 6.4.3.3.

6.4.4.2 The specification of thickness should meet the requirements of Table 4.

Table 4 Thickness Specification

Parameter	*Specification*			*Test Condition/Technique*
	Average (μm)	*Tolerance (%)*	*Uniformity (%)*	
Thickness	2–30	±10	<10	Fourier transform infrared (FT-IR)#1 measurement/SEMI MF95

#1 A method for measuring the thickness of epitaxial layer.

6.4.5 *Surface Defect*

6.4.5.1 *Surface Killer Defect*

6.4.5.1.1 The surface killer defect of epitaxial layer should meet the requirements of Table 5.

Table 5 Surface Killer Defect Specification

Parameter	*Specification*	*Test Condition/Technique*	*Note*
Total usable area (%)	≥90	Determine by a method agreed upon between the supplier and the customer.	#1

#1 The parameter of total usable area is defined in § 4.2.20, and it is calculated by 2 mm × 2 mm grid size. The measurement area is the entire wafer surface except for 3 mm EE area.

6.4.5.2 *Surface Scratch*

6.4.5.2.1 The surface scratch of epitaxial layer should meet the requirements of Table 6.

Table 6 Surface Scratch Specification

Parameter	*Specification*	*Test Condition/Technique*	*Note*
Surface scratch	cumulative length <1× wafer diameter	High intensity light, unaided eye/SEMI MF523	#1

#1 The measurement of areas is the entire wafer surface.

6.4.6 *Surface Roughness*

6.4.6.1 The surface roughness of epitaxial layer should meet the requirements of Table 7.

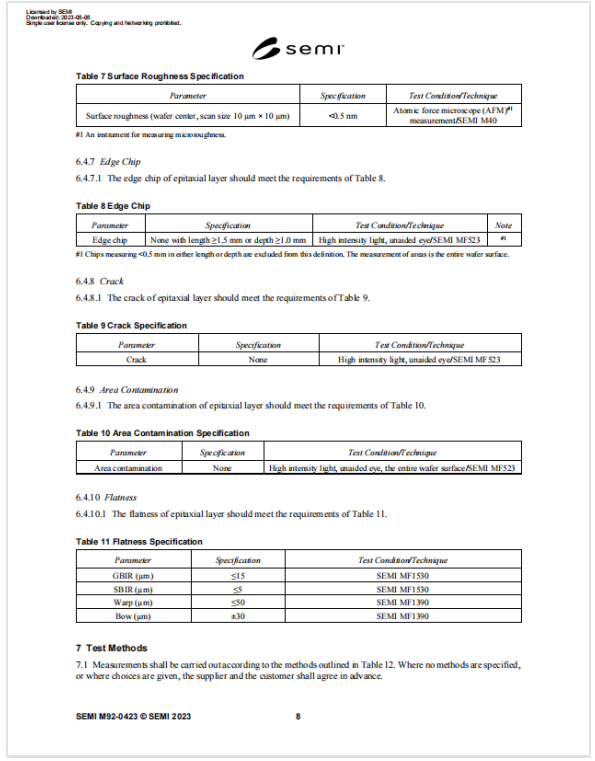


Table 7 Surface Roughness Specification

Parameter	*Specification*	*Test Condition/Technique*
Surface roughness (wafer center, scan size 10 μm × 10 μm)	<0.5 nm	Atomic force microscope (AFM)#1 measurement/SEMI M40

#1 An instrument for measuring microroughness.

6.4.7 *Edge Chip*

6.4.7.1 The edge chip of epitaxial layer should meet the requirements of Table 8.

Table 8 Edge Chip

Parameter	*Specification*	*Test Condition/Technique*	*Note*
Edge chip	None with length ≥1.5 mm or depth ≥1.0 mm	High intensity light, unaided eye/SEMI MF523	#1

#1 Chips measuring <0.5 mm in either length or depth are excluded from this definition. The measurement of areas is the entire wafer surface.

6.4.8 *Crack*

6.4.8.1 The crack of epitaxial layer should meet the requirements of Table 9.

Table 9 Crack Specification

Parameter	*Specification*	*Test Condition/Technique*
Crack	None	High intensity light, unaided eye/SEMI MF523

6.4.9 *Area Contamination*

6.4.9.1 The area contamination of epitaxial layer should meet the requirements of Table 10.

Table 10 Area Contamination Specification

Parameter	*Specification*	*Test Condition/Technique*
Area contamination	None	High intensity light, unaided eye, the entire wafer surface/SEMI MF523

6.4.10 *Flatness*

6.4.10.1 The flatness of epitaxial layer should meet the requirements of Table 11.

Table 11 Flatness Specification

Parameter	*Specification*	*Test Condition/Technique*
GBIR (μm)	≤15	SEMI MF1530
SBIR (μm)	≤5	SEMI MF1530
Warp (μm)	≤50	SEMI MF1390
Bow (μm)	±30	SEMI MF1390

7 Test Methods

7.1 Measurements shall be carried out according to the methods outlined in Table 12. Where no methods are specified, or where choices are given, the supplier and the customer shall agree in advance.

Documents in Work

SEMI Draft Document (Published): M092-0423 4H-SiC Homoepitaxial Wafer Specification 4H-SiC同质外延片标准

7.2 Given the lack of standard reference materials, it is advisable that the supplier and the customer exchange samples to cross calibrate their measurement instruments and procedures.

Table 12 Parameter and Recommended Test Method

Category	*Parameter*	*Test Method*
Substrate	Polytype	None as yet
	Conductivity Type (Dopant)	None as yet
	Diameter	SEMI MF2074
	Thickness	SEMI MF533 or SEMI MF1530
	Surface Orientation	SEMI MF26 (Method A)
	Resistivity	SEMI MF673
	Primary Flat Length	SEMI MF671
	Primary Flat Orientation	SEMI MF847
	Secondary Flat Length	SEMI MF671
	Secondary Flat Orientation	SEMI MF847
	Micropipe Density	Determine by a method agreed upon between the supplier and the purchaser
	Dislocation Etch Pit Density	KOH Etched Surface, SEMI M83 and SEMI M81 or by a method agreed upon between the supplier and the purchaser
	GBIR	SEMI MF1530
	SBIR	SEMI MF1530
	Warp	SEMI MF1390
	Bow	SEMI MF1390
Buffer layer	Polytype	None as yet
	Conductivity Type (Dopant)	None as yet
	Carrier Concentration	None as yet
	Thickness	None as yet
Epitaxial layer	Polytype	None as yet
	Conductivity Type (Dopant)	None as yet
	Carrier Concentration	SEMI MF1392 or equivalent
	Thickness	SEMI MF95
	Surface killer defect	Determine by a method agreed upon between the supplier and the customer
	Surface scratch	SEMI MF523
	Surface roughness	SEMI M40
	Edge chip	SEMI MF523
	Crack	SEMI MF523
	Area contamination	SEMI MF523
	GBIR	SEMI MF1530
	SBIR	SEMI MF1530
	Warp	SEMI MF1390
	Bow	SEMI MF1390

8 Sampling

8.1 Unless otherwise specified, ASTM E122 shall be used to define the sampling plan. When so specified, appropriate sample sizes shall be selected from each lot in accordance with ANSI/ASQ Z1.4. Each quality characteristic shall be assigned an acceptable quality level (AQL) or lot total percent defective (LTPD) value in accordance with ANSI/ASQ Z1.4 definitions for critical, major and minor classifications. If desired and so specified in the contract or order, each of these classifications may alternatively be assigned cumulative AQL or LTPD values. Inspection levels shall be agreed upon between the supplier and the customer.

9 Certification

9.1 Upon request of the customer in the contract or order, a manufacturer's or supplier's certification that the material was manufactured and tested in accordance with this Specification, together with a report of the test results, shall be furnished at the time of shipment.

9.2 The customer and supplier may agree that the material shall be certified as 'capable of meeting' certain requirements. In this context, 'capable of meeting' shall signify that the supplier is not required to perform the appropriate tests in §§ 6 and 7, however, if the customer performs the test and the material fails to meet the requirement, the material may be subject to rejection.

10 Packing and Labeling

10.1 Special packing and marking requirements shall be subject to agreement between the supplier and the customer. Otherwise, all the wafers shall be handled, inspected, and packed in such a manner as to avoid chipping, scratches, and contamination in accordance with the best industry practices to provide sample protection against damage during shipment.

10.2 The wafers shall be identified by appropriately labeling the outside of each box or other container and each subdivision thereof in which it may reasonably be expected that the wafers will be stored prior to further processing. Identification shall include as a minimum the nominal diameter, conductive dopant (structure), quantity, and lot number.

11 Related Documents

11.1 *SEMI Standards and Guidelines*

SEMI MF154 — Guide for Identification of Structures and Contaminants Seen on Specular Silicon Surfaces

SEMI MF928 — Test Method for Edge Contour of Circular Semiconductor Wafers and Rigid Disk Substrates

SEMI T5 — Specification for Alphanumeric Marking of Round Compound Semiconductor Wafers

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Documents Request Inactive

SEMI Draft Document: None

Documents Request Abolished

SEMI Draft Document: None

THANK YOU

STANDARDS